CLAIMS:

1. A method of de-skewing a plurality of serial data signals respectively outputted from a plurality of data lanes, the method comprising:

simultaneously feeding a test signal to inputs of the plurality of data lanes and monitoring respective outputs thereof;

respectively detecting a predetermined data element of the test signal outputted from each of the plurality of data lanes;

measuring respective elapsed times from the detection of the predetermined data element outputted from each of the plurality of data lanes to the detection that the predetermined data element has been outputted from all of the plurality of data lanes; and

de-skewing the plurality of serial data signals by respectively delaying them in accordance with their respective measured elapsed times.

2. The method of claim **1**, wherein the test signal comprises the predetermined data element, a lane identifier, and a predetermined number of additional data symbols, the predetermined data element comprising a predetermined data character.

3. The method of claim **1**, wherein the elapsed times are measured by a plurality of lane tolerance counters, each counter initiating counting upon the detection

of the predetermined data element in its data lane and each counter stopping counting upon the detection that the predetermined data element has been outputted from all of the plurality of data lanes.

4. The method of claim **1**, wherein the plurality of serial data signals are respectively delayed by a plurality of registers.

5. The method of claim **3**, wherein the plurality of serial data signals are respectively delayed by a plurality of registers.

6. The method of claim **5**, wherein the amount of delay of each data signal is selected by a respective multiplexer connected to the plurality of registers, each multiplexer being controlled by its' respective counter.

7. The method of claim **1**, further comprising detecting elapsed time from a first detection of the predetermined data element on any of the plurality of data lanes and declaring a de-skewing failure upon the detected elapsed time reaching a predetermined amount before the predetermined data element has been detected on all of the plurality of data lanes.

8. An apparatus for de-skewing a plurality of serial data signals respectively outputted from a plurality of data lanes, the apparatus comprising:

a test signal generator simultaneous feeding a test signal to inputs of the plurality of data lanes;

a plurality of data element detectors respectively connected to outputs of the plurality of data lanes to respectively detect a predetermined data element of the test signal outputted from each of the plurality of data lanes;

a control state machine connected to the plurality of data element detectors to detect that the predetermined data element of the test signal outputted from each of the plurality of data lanes has been detected by all of the data element detectors;

a plurality of elapsed time detectors to detect respective elapsed times from the detection by the data element detectors of the predetermined data element outputted from each of the plurality of data lanes to the detection by the control state machine that the predetermined data element has been outputted from all of the plurality of data lanes; and

a plurality of time delay units respectively connected to the plurality of elapsed time detectors to respectively delay the plurality of serial data signals in accordance with the detected elapsed times of their respective elapsed time detectors.

9. The apparatus of claim 8, wherein the test signal comprises the predetermined data element, a lane identifier, and a predetermined number of additional

data symbols, the predetermined data element comprising a predetermined data character.

10. The apparatus of claim **8**, wherein the plurality of elapsed time detectors respectively comprise a plurality of lane tolerance counters, each counter initiating counting upon the detection of the predetermined data element in its data lane by its respective data element detector and each counter stopping counting upon the detection that the predetermined data element has been outputted from all of the plurality of data lanes as detected by the control state machine.

11. The apparatus of claim **8**, wherein the plurality of time delay units respectively comprise a plurality of registers.

12. The apparatus of claim **11**, wherein the plurality of time delay units respectively comprise a plurality of registers.

13. The apparatus of claim **12**, further comprising a plurality of multiplexers respectively connected to the plurality of registers and plurality of counters, each multiplexer selectively determining the amount of delay of its respective data signal in accordance with an output from its' respective counter.

14. The apparatus of claim 8, wherein the control state machine monitors elapsed time from a first detection of the predetermined data element on any of the plurality of data lanes by one of the plurality of elapsed time detectors and declares a de-skewing failure upon the monitored elapsed time reaching a predetermined amount before the predetermined data element has been detected on all of the plurality of data lanes by the plurality of data element detectors.

15. The apparatus of claim 10, further comprising a plurality of sticky flip-flops respectively disposed between said plurality of data element detectors and their respective counters.

16. A program storage device, readable by machine and tangibly embodying a program of instructions executable by the machine to perform a method of de-skewing a plurality of serial data signals respectively outputted from a plurality of data lanes, the method comprising:

simultaneously feeding a test signal to inputs of the plurality of data lanes and monitoring respective outputs thereof;

respectively detecting a predetermined data element of the test signal outputted from each of the plurality of data lanes;

measuring respective elapsed times from the detection of the predetermined data element outputted from each of the plurality of data lanes to the

detection that the predetermined data element has been outputted from all of the plurality of data lanes; and

de-skewing the plurality of serial data signals by respectively delaying them in accordance with their respective measured elapsed times.

17. The device of claim **16**, wherein the test signal comprises the predetermined data element, a lane identifier, and a predetermined number of additional data symbols, the predetermined data element comprising a predetermined data character.

18. The device of claim **16**, wherein the elapsed times are measured by a plurality of lane tolerance counters, each counter initiating counting upon the detection of the predetermined data element in its data lane and each counter stopping counting upon the detection that the predetermined data element has been outputted from all of the plurality of data lanes.

19. The device of claim **16**, wherein the plurality of serial data signals are respectively delayed by a plurality of registers.

20. The device of claim **18**, wherein the plurality of serial data signals are respectively delayed by a plurality of registers.

21. The device of claim **20**, wherein the amount of delay of each data signal is selected by a respective multiplexer connected to the plurality of registers, each multiplexer being controlled by its' respective counter.

22. The device of claim **16**, further comprising detecting elapsed time from a first detection of the predetermined data element on any of the plurality of data lanes and declaring a de-skewing failure upon the detected elapsed time reaching a predetermined amount before the predetermined data element has been detected on all of the plurality of data lanes.

SERDES into the core clock domain. FIG. 3 is a block diagram of the receive architecture of such an arrangement.

As shown in FIG. 3, the SERDES 310 generates the clock (RXC) and data (RXD) inputs to the PHY (Physical Interface) block 320. All of the elements in the PHY 320 operate in the RXC domain. Due to the potential instability of the RXC domain, caused by the clock being recovered from the serial data stream inputted to the SERDES, it is desirable to transition the receive data into the core clock domain. The PHY 320 controls the write function into the elastic buffer 330 which is employed to transition the data stream to the core clock domain from the RXC domain. This is required because of the frequency deviance of the oscillators used for the core clocks that generate the transmit clock and data. The receiver 340, operating in the core clock domain, extracts the data from the elastic buffer and performs all of the necessary checks prior to storing the packet in a memory. The elastic buffer serves as a mechanism for transitioning the link data stream into the core clock domain.

As noted above, in order to increase network performance, multi-lane serial links are used. These lanes are essentially individuals serial links which are operating a parallel and in synchronism. Packets are byte striped across the serial links and subsequently reassembled. FIG. 4 is a block diagram of such a multi-lane receive architecture.

As shown in FIG. 4, N+1 physical interface blocks PHY-0 to PHY-N are respectively connected to elastic buffers 0 to N. Operating the multiple links in parallel